

IN THE CLAIMS

Please cancel claims 1-16 without prejudice.

Please add new claims 17-40 that follow below.

1 1-16. (Cancelled)

1 17. (New) A method of forming an integrated
2 circuit package, comprising:
3 providing a package housing having a first plurality of
4 bonding pads located on a first bond shelf, the first bond
5 shelf having a first edge;
6 forming a first conductive strip along the first edge
7 of the first bond shelf, the first conductive strip wrapping
8 around the edge of the first bond shelf from at least one of
9 the first plurality of bonding pads on the first bond shelf
10 to a first conductor under the first bond shelf; and,
11 removing a portion of the first conductive strip.

1 18. (New) The method as recited in claim 17,
2 wherein
3 the first conductive strip is formed by plating a
4 conductive material onto the first edge.

1 19. (New) The method as recited in claim 17,
2 wherein

3 the first conductor under the first bond shelf is a
4 power bus.

1 20. (New) The method as recited in claim 17,
2 wherein
3 the first conductor under the first bond shelf is
4 a routing trace.

1 21. (New) The method as recited in claim 17,
2 wherein
3 the portion of the first conductive strip is removed by
4 drilling a portion of the first bond shelf.

1 22. (New) The method as recited in claim 21,
2 wherein
3 the portion drilled in the first bond shelf is a
4 notch.

1 23. (New) The method as recited in claim 17,
2 wherein
3 the portion of the first conductive strip is removed by
4 etching away a portion of the first conductive
5 strip of the first bond shelf.

1 24. (New) The method as recited in claim 17,
2 wherein

3 the package housing is provided by
4 forming a first conductive layer on a first
5 dielectric substrate,
6 placing a second dielectric substrate on the first
7 conductive layer of the first dielectric substrate, the
8 second dielectric substrate having a second conductive
9 layer, and
10 etching the second conductive layer to form the
11 first plurality of bonding pads.

1 25. (New) The method as recited in claim 24,
2 wherein

3 the first conductive layer forms the first
4 conductor under the first bond shelf.

1 26. (New) The method as recited in claim 24,
2 wherein

3 the etching of the second conductive layer to further
4 form a second conductor, and

5 the package housing has a second plurality of bonding
6 pads located on a second bond shelf, the second bond shelf
7 having a second edge, the package housing is further
8 provided by

9 placing a third dielectric substrate on the
10 second conductive layer of the second dielectric

11 substrate, the third dielectric substrate having a
12 third conductive layer, and
13 etching the third conductive layer to form a
14 second plurality of bonding pads,
15 and
16 the method further includes
17 forming a second conductive strip along the second edge
18 of the second bond shelf, the second conductive strip
19 wrapping around the second edge of the second bond shelf
20 from at least one of the second plurality of bonding pads on
21 the second bond shelf to the second conductor under the
22 second bond shelf.

1 27. (New) The method as recited in claim 26,
2 wherein
3 the second conductive layer forms the second
4 conductor under the second bond shelf.

1 28. (New) The method as recited in claim 26,
2 wherein
3 the second conductive strip is formed by plating a
4 conductive material onto the second edge.

1 29. (New) The method as recited in claim 26,
2 wherein

3 the second conductor under the second bond shelf
4 is a power bus.

1 30. (New) The method as recited in claim 26,
2 wherein
3 the second conductor under the second bond shelf
4 is a routing trace.

1 31. (New) A method of forming an integrated circuit
2 package, comprising:
3 providing a package housing having a first bond shelf
4 with a top surface and an inside surface;
5 forming a conductive material along the inside surface
6 of the first bond shelf, a first portion of the conductive
7 material wrapping around from the inside surface onto the
8 top surface of the first bond shelf to form at least one of
9 a first plurality of bonding pads on the top surface of the
10 first bond shelf; and,
11 removing a second portion of the conductive material
12 along the inside surface of the bond shelf to form a pair of
13 separate conductive strips along the inside surface of the
14 bond shelf.

1 32. (New) The method as recited in claim 31, wherein
2 the conductive material is formed along the inside

3 surface by plating a conductive material onto the inside
4 surface.

1 33. (New) The method as recited in claim 31, wherein
2 the second portion of the conductive material is
3 removed by
4 drilling a portion of the first bond shelf.

1 34. (New) The method as recited in claim 33, wherein
2 the portion drilled in the first bond shelf is a
3 notch.

1 35. (New) The method as recited in claim 31, wherein
2 the second portion of the conductive material is
3 removed by etching away a portion of the conductive material
4 from the inside surface of the first bond shelf.

1 36. (New) A method of forming an integrated circuit
2 package, comprising:
3 providing a package housing having a rectangular bond
4 shelf with a rectangular top surface and an inside surface
5 perpendicular with the top surface, the bond shelf having a
6 first plurality of bonding pads located on the top surface;
7 forming a conductive material along the side surface of
8 the bond shelf, a first portion of the conductive material

9 wrapping around from the inside surface onto the top surface
10 of the bond shelf to couple to at least one of the first
11 plurality of bonding pads on the top surface of the bond
12 shelf; and,

13 removing a second portion of the conductive material
14 along the inside surface of the bond shelf to form a pair of
15 separate conductive strips along the inside surface of the
16 bond shelf.

1 37. (New) The method as recited in claim 36, wherein
2 the conductive material is formed along the inside
3 surface by plating a conductive material onto the inside
4 surface of the bond shelf.

1 38. (New) The method as recited in claim 36, wherein
2 the second portion of the conductive material is
3 removed by
4 drilling a portion of the bond shelf.

1 39. (New) The method as recited in claim 38, wherein
2 the portion drilled in the bond shelf is a notch.

1 40. (New) The method as recited in claim 36, wherein
2 the second portion of the conductive material is
3 removed by etching away a portion of the conductive material

4 from the inside of the first bond shelf.